Design of Bandgap Reference Circuit for Driving Resistance Load with Low Impedance

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Abstract— This paper describes the design of a bandgap Reference for driving low impedance, simulated in 0.35µm CMOS technology. The circuit generates a reference voltage of 1.23V and has a temperature coefficient of 0.02mV/K at 27C. It can operate with supply voltages between 2.5V and 6V and between 0C and 100C. It has a PSRR of 41dB under normal operating conditions. This circuit works in a current feedback mode, and it generates its own reference current, resulting in a stable operation. A startup circuit is required for successful operation of the system. Variation of the reference voltage with RL from 40_ to 200_ at 27°C_is 4mV.

Index Terms— Proportional To Absolute Temperature (PTAT), Conversely proportional To Absolute Temperature (CTAT), Bandgap Referenc (BGR), Temperature Coefficient (TC).

1 INTRODUCTION

Many analog circuits require voltage references, such as A/D and D/A converters. A voltage reference must be, inherently, well-defined and insensitive to temperature, power supply and load variations. The resolution of an A/D or D/A converter is limited by the precision of its reference voltage over the circuit's supply voltage and operating temperature ranges. The bandgap voltage reference is required to exhibit both high power supply rejection and low temperature coefficient, and is probably the most popular high performance voltage reference used in integrated circuits today.

By definition a bandgap reference is a voltage reference of which the output voltage is referred to the bandgap energy of the used semiconductor. The first bandgap reference was proposed by Robert Widlar in 1971 [1].

The working principle of a bandgap voltage reference can be illustrated by Fig1. Since VBE decreases approximately linear with temperature while VT increases linearly with temperature, a low-temperature-dependence VREF can be obtained by scaling up VT and summing it with VBE.

As a well-established reference generator technique, bandgap reference is most popular for both Bipolar and CMOS technologies. The principle of the bandgap circuits relies on two groups of diode-connected BJT transistors .

running at different emitter current densities. By canceling the negative temperature dependence of the PN junctions in one group of transistors with the positive temperature dependence from a PTAT (proportional-to-absolute-temperature) circuit which includes the other group of transis

tors, a fixed DC voltage which doesn't change with temperature is generated. This voltage is typically 1.26 volts, which is approximately the band gap of silicon. [2][3]

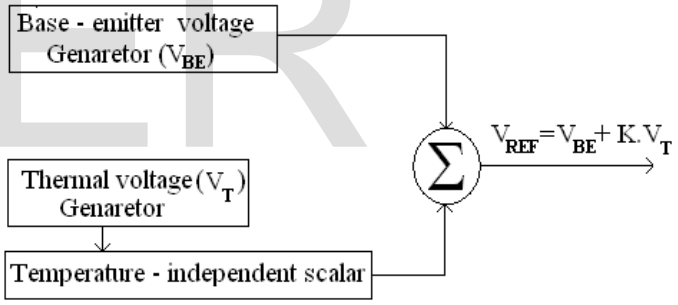

Fig1.Concept of bandgap Voltage Reference

The outline of this paper is as follows: in section II circuit description is presented. Section III presents circuit analysis units. In the section V, we demonstrated simulation result. The results were obtained by simulation produce in a 0.35 µm process.

2 CIRCUIT DESCRIPTION

Adding two voltages that have temperature coefficients of opposite sign with suitable multiplication constants generates a reference voltage. The resulting voltage obtained is independent of temperature. The diode voltage drop across the base-emitter junction, VBE, of a Bipolar Junction Transistor (BJT) changes Complementary to Absolute Temperature (CTAT) [4]. Whereas if two BJTs operate with unequal current densities, then the difference in the base emitter voltages, _VBE, of the transistors is found to be Proportional to Absolute Temperature (PTAT). The PTAT relationship is given by [5],

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$$\Delta V_{BE} = V_T \ln m; \qquad V_T = kT/q \qquad (1)$$

where, k is Boltzmann's constant, T is the absolute temperature, q is the electron charge and m is the ratio of the current densities of the two BJTs. The PTAT voltage may be added to the CTAT voltage with suitable weighting constants to obtain a constant reference voltage. By using a supply independent current source, a current Iss is passed through BJT A. The same current Iss flows through m transistors connected in parallel, identical to A. Thus the current density of A is m times the current density of the m BJTs identical to A, connected in parallel. The voltages at node X and Y are maintained at the same value, VBE using a feedback network through a differential amplifier. This results in a voltage of ΔVBE, across the resistor R1. The voltages VBE and ΔVBE are added to obtain the reference voltage. The circuit also requires a startup circuit since there exists a stable state at which no current flows through the circuit. The startup circuit forces the transistors to turn on and the circuit to operate at its other stable state to generate the reference voltage. It should be noted that an ideal BJT is not available in CMOS technology.

3 Circuit Analysis

3.1 Main Core of Circuit

The bandgap reference voltage is generated by adding the base emitter voltage, VBE, of a BJT to the difference in base emitter voltage, ΔVBE of BJTs with a ratio of current density m. In order to generate a stable circuit, it is necessary to keep the BJT in the exponential region.

The change of the voltage of reference node is made possible by adding variable resistor in the base of Q1 and Q2 transistors. Ideally, the error amplifier has a high voltage gain A, and therefore VX=VY can be achieved, when VDSTP1=VDSTP2 can be easily obtained to provide a very good current matching by M1 and M2. VREF can be generated by this structure without the need of an extra current branch.

Both power consumption and errors can be reduced effectively.

A pnp BJT is made using the n-well normally associated with a PFET [4], the p substrate behaving as the collector. The OPAMP provides the base voltage to the transistors which are connected as current mirrors. By selecting the value of R1 and current Iss, the circuit may be designed to operate at the desired operating point. The value of R1 is given by,

$$R1 = \Delta V_{BE} / I_{SS} \qquad (2)$$

Since the same current Iss flows through R2, the voltage at the output reference voltage nodes is given by,

$$V_{ref} = V_{BE} + \Delta V_{BE} \cdot \frac{R_1}{R_2} \qquad (3)$$

Thus by selecting the value of R2 the weighting constant maybe set. This arrangement provided an elegant arrangement to generate the reference voltage while conserving voltage headroom. The circuit has a stable operating point at which no current to flows through it. An arrangement must be made to force the saturation when the supply is turned on. This function is carried out by the startup circuit.

The voltages X and Y are fixed by feedback; hence result the VREF is given by,

$$V_{ref} = I_{ss}.R2 + V_{BE} \qquad (4)$$

$$V_{ref} = \frac{\Delta V_{BE}}{R1}.R2 + V_{BE} \qquad (5)$$

$$V_{ref} = \frac{R2}{R1}.V_T.\ln m + V_{BE} \qquad (6)$$

In the order achieve a zero temperature coefficient; the following equation must be satisfied.

$$\frac{\partial V_{ref}}{\partial T} = \frac{R2}{R1}\ln m.\frac{\partial V_T}{\partial T} + \frac{\partial V_{BE}}{\partial T} \qquad (7)$$

$$\frac{\partial V_{ref}}{\partial T} = 0 \qquad (8)$$

$$\frac{R2}{R1}\ln m.\frac{\partial V_T}{\partial T} = -\frac{\partial V_{BE}}{\partial T} \qquad (9)$$

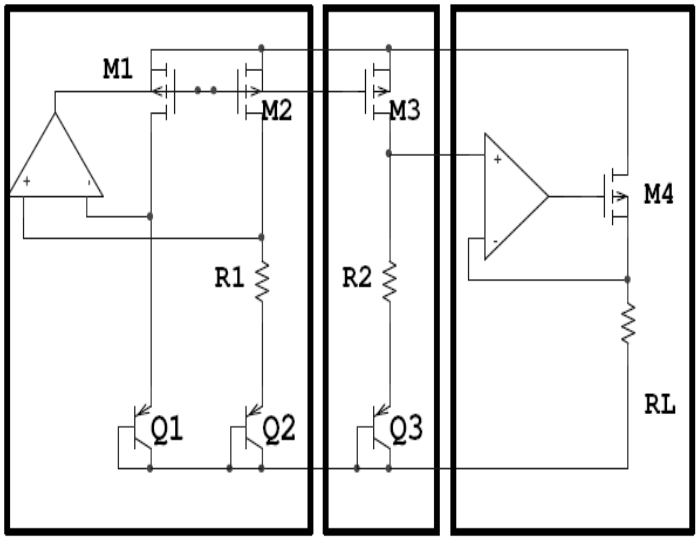

Fig. 2: Schematic of Bandgap Reference Circuit showing the supply independent current source, generation of reference voltage and driving low Impedance block

The equation shows that R1, R2 and m affect on the TC of Vref. m is the ratio of the surface of Q1 and Q2 transistors. Because layouts on both BJTs and resistors should be well planned and designed so that consistent performance can be maintained with minimum need of trimming in mass productions. Better matching can be achieved by a common-centroid layout [6],[7]. However a large value of N is not preferred as the separation of devices increases, and this will introduce more errors. Moreover, as shown in (8) there is no signification increase on the ln(m) function when m increases.

For the resistor layout, common-centroid layout should be also used to obtain better matching [7]. Polysilicon is a better material than diffusion since its tempco is low. An even better material is high-resistive polysilicon, since it has a negative tempco. We used in the simulation.

As mentioned above, the amplitude of R1 and m are set before. Therefore only R2 is affected in the thermal characteristic.

3.2 Opamp

The OPAMP was used to maintain equal node voltages and provide a feedback to maintain the drain currents constant and insensitive to supply variations. A high gain of the OPAMP would result in better voltage tracking of nodes X and Y (Fig2). The common mode voltages play an important role in determining the OPAMP topology. The input common mode was determined by the base emitter voltage of the BJT. In order to meet the input common mode condition an active current mirror circuit with a PMOS driver was selected.

The output common mode voltage corresponds to the gate voltage of the current mirror transistors. A second stage was added to the OPAMP to increase gain and shift the common mode voltage up by using an NMOS driver. The NMOS driver only provided an output common mode of about 0.4 V. By adding a diode-connected transistor to the second stage, the output voltage was pushed up to about 1.3 V without any effect on the gain of the stage. The voltage drop across the diode connected transistor is about 1.2 V corresponding to VTH + VDSAT. The gain of each of the stages of the OPAMP is given by

$$A=gm.Ro \qquad (9)$$

Where, Av is the gain, gm is the transconductance of the driving transistor and RO is the effective output resistance at the output node.

3.3 Startup circuit

Transistors TN1, TN2, TN3 and TP4 constitute the startup circuit. Initially all the transistors start off in off state. The voltage at the gate of TN1 is low and so it remains in off state. TP4 being diode connected is always on and so the transistor TN2 turns on forcing the drain to a low value. The current mirror stack turns on and the gate voltage of TN1 rises and it starts to conduct. At this point there is a competition between the output of the amplifier TP6 and TN2 for the current source load. TN2 is designed to be a weak transistor so the amplifier takes control of the current mirror gate (Fig3).

When the bandgap voltage is high enough (~1V) the transistor TN1 turns on. TN1 in linear region has to compete with TN2 in saturation so it is designed to be a big transistor. It draws all the current from TP2 and the base voltage of TN2 falls till it turns off. In this state the gate voltage at TN2 is about 0.6 V. This is high enough for the transistor TN1 to be conduct slightly. A diode connected transistor TN3 is added to increase the threshold voltage at the gate of TN3 to turn off. The transistor TP4 is designed to be a weak device so that low current flows through the parasitic path when the circuit is in full operation.

3.4 Driving low Impedance block

The Opamp_was used to maintain equal node voltages. A high gain of the OPAMP would result in better voltage tracking of nodes. In fact, this opamp and M4 (Fig2) transistor provide sufficient current for low Impedances without effecting over the main characteristic of bandgap reference

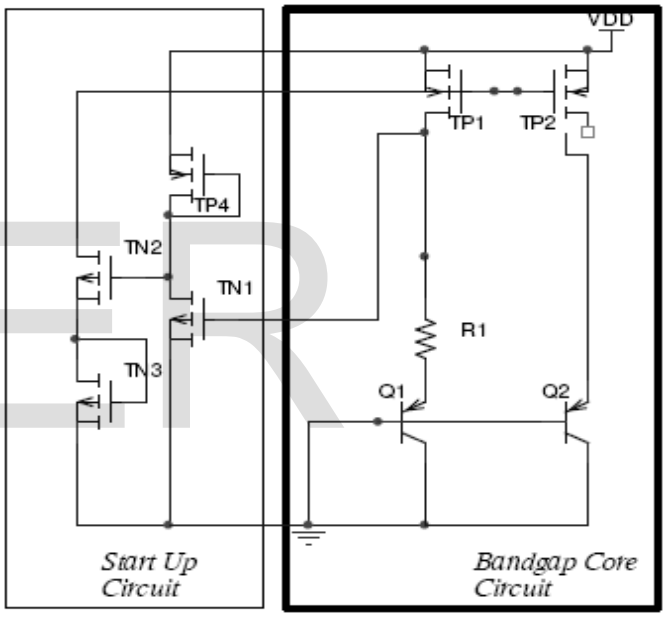

Fig. 3: Schematic of Bandgap core Circuit with startup

4 Results

The bandgap reference voltage gives a voltage of 1.23V when adjusted to have a zero temperature coefficient at 27C. Fig4 shows the result of the simulation. As can be seen an overall temperature coefficient of 0.01mV/K is obtained between 0°C and 100°C. The response it worse for temperatures from 60-100°C with a temperature coefficient of 0.024mV/K. Below these temperatures the temperature coefficient is 0.016mV/K.

Fig 5 shows variation of IL when temperature changes between 0°C to 100°C. Temperature coefficient of 0.0005mA/K is obtained.

Fig 6 shows the variation when the supply voltage is varied from 2.5V to 6V. The relative variation is 0.41% at 27C.

Fig 7 shows the variation when the RL is varied from 40Ω to 200 Ω. The relative variation is 0.325%. at 27C.

5 CONCLUSION

A bandgap reference with a current feedback mode has been designed to drive low Impedance. The circuit uses no external current sources and is designed to have a zero temperature coefficient at 27°C. The design is simulated with 0.35µm CMOS process. Table 1 shows the summary of performance of proposed circuit. The output voltage is 1.2364V at the nominal operating condition of 27°C temperature and 3.3V supply voltage. It has a temperature coefficient of 0.01mV/K from 0-100°C.

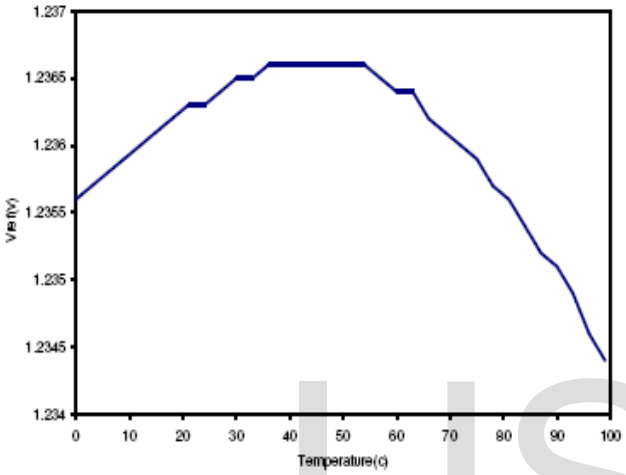

Fig 4: Variation of bandgap reference with temperature

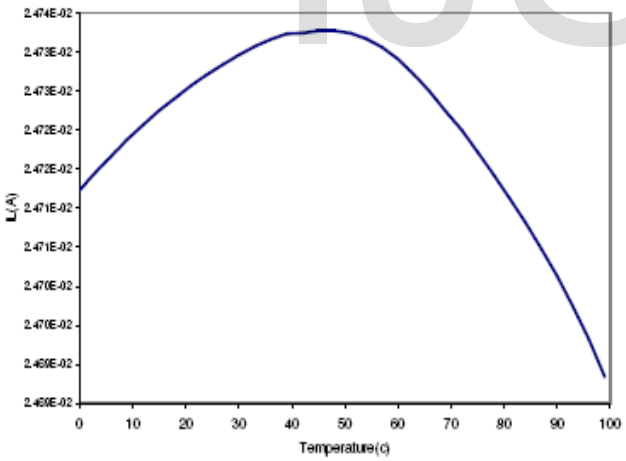

Fig 5: Variation of current load with temperature at Vdd=3.3v

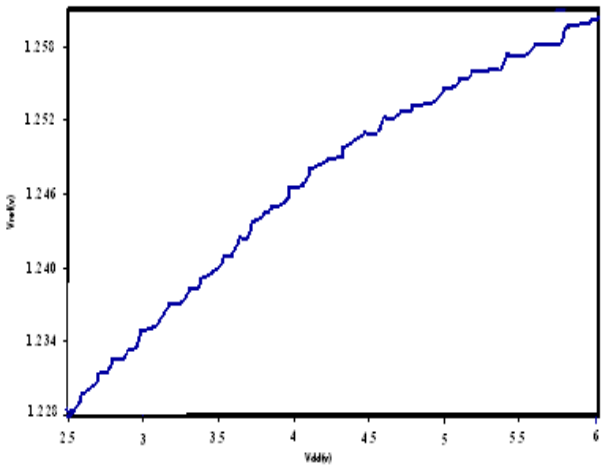

Fig 6: Variation of the reference voltage with supply voltage at 27C

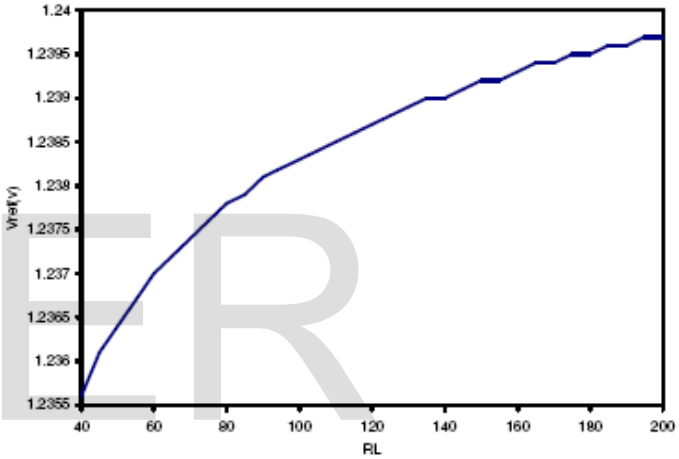

Fig 7: Variation of the reference voltage with RL at 27C

TABLE1: SUMMARY OF PERFORMANCE

	With RL=50 Ω
Technology (µm)	0.35
Supply voltage range (Volt)	2.5-6
VREF (Volt)T=27°C	1.2364
PSRR (dB)	41
Temperature coefficient (ppm/°C) Vdd=3.3v	9.85
Integrated noise (_V/sqrt Hz)	0.319

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